An EMC-oriented VHDL-AMS Simulation Methodology for Dynamic Current Activity Assessment

Richard Perdriau\textsuperscript{a,b,\ast}, Mohamed Ramdani\textsuperscript{a}, Jean-Luc Levant\textsuperscript{c}, Eric Tinlot\textsuperscript{c} and Anne-Marie Trullemans-Anckaert\textsuperscript{b}

\textsuperscript{a}ESEO - 4, rue Merlet-de-la-Boulaye - BP 926 - 49009 Angers Cedex 01 - France
\textsuperscript{b}DICE - Laboratoire de Microélectronique - Université Catholique de Louvain Place du Levant, 3 - 1348 Louvain-la-Neuve - Belgium
\textsuperscript{c}ATMEL - La Chantrerie - Route de Gachet - 44000 Nantes - France

Abstract

Dynamic current activity extraction plays a very important role in estimating the electromagnetic compatibility of integrated circuits. For that purpose, the Integrated Circuit Electromagnetic Model (ICEM) is being developed by the International Electrotechnical Commission (IEC). This article introduces a mixed-mode simulation methodology, based on the VHDL-AMS language, which dramatically reduces simulation times while taking into account various circuit activities. The use of such a methodology in the case of SRAM memories is described, allowing the definition of an ICEM-compatible intellectual-property (IP) dynamic activity model aimed at emission level prediction.

Key words: Electromagnetic compatibility, ICEM, VHDL-AMS, modelling, simulation, memories, prediction

1 Introduction

When designing complex integrated circuits such as microcontrollers ($\mu$C), extreme care must be taken about their compliance to electromagnetic compatibility (EMC) rules; in fact, the later these rules are taken into account

\textsuperscript{\ast} Corresponding author. Tel. (33/0) 2 41 86 67 03 - Fax. (33/0) 2 41 87 99 27
Email address: richard.perdriau@eseo.fr (Richard Perdriau).
URL: http://www.eseo.fr/\textasciitilde rperdriau (Richard Perdriau).

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in the design phase, the more non-recurrent engineering (NRE) costs will increase due to foundry costs. Moreover, according to the MEDEA+ EDA roadmap [8], despite ever decreasing supply voltages (0.3 V in 2013), conducted emission levels should slightly increase (100 µV in 2013, with 25 GHz system clock, instead of 90). Therefore, a methodology allowing the designer to predict conducted emission levels before sending the design to the foundry becomes compulsory.

This explains the emergence of various new models, including the recent Integrated Circuit Electromagnetic Model (ICEM) proposal [9], represented in figure 1.

ICEM helps predicting perturbations generated by the IC on power supply lines. The model includes passive elements representing the internal capacitors (metal and MOS) $C_b$, the bonding ($R_{VDD}, L_{VDD}, R_{VSS}, L_{VSS}$), the internal decoupling capacitor $C_d$, and the package ($R_{PVDD}, L_{PVDD}, R_{PVSS}, L_{PVSS}$), along with an equivalent current generator $I_b$ modeling internal activity. A methodology for obtaining equivalent schematics of the passive power network has already been introduced in [5] and developed in [6]; therefore, this article only deals with the active part of the model, i.e. $I_b$ extraction and modeling. This current generator is independent from the passive elements of the model; therefore, predicting conducted emission becomes possible by modifying the passive network as a function of the package (and the printed circuit board, which is included as well but not represented).

The first idea coming to mind in order to obtain $I_b$ is to perform a transistor-level simulation on the complete netlist, using SPICE-like tools. However, many microcontrollers include on-chip SRAM, Flash EPROM and/or EEPROM. These memory blocks often contain many more transistors than the CPU core itself; hence, simulating millions of transistors at SPICE level would be tedious and time-consuming. Moreover, EMC studies do not require as much accuracy as the one provided by these simulations; indeed, results might be acceptable when the discrepancy between simulation results and measurements is as high as 20%.

On the contrary, many authors have already demonstrated the advantages of behavioural simulation models over structural ones for complex systems, mainly in terms of simulation time. For that purpose, many high-level, mixed-signal languages have been developed in the last decade, including HDL-A, MAST and more recently VHDL-AMS and Verilog-AMS.

Nonetheless, as is well known, microcontroller core models are written in purely digital VHDL or Verilog in order to be synthesised; in addition, VITAL (VHDL Initiative Towards ASIC Libraries) behavioural models of memory blocks are often available. The VITAL standard (IEEE 1076.4-1995, enhanced in 1999) allows (among other features) memory read/write operations to be simulated in VHDL, including timings and path delays. The use of a similar, compatible modelling language seems thus to match the requirements of a global simulation.

VHDL-AMS, described in [1], is a mixed-signal, multi-technology extension
to VHDL, covering various domains including electronics, mechanics and optics. Moreover, purely digital VHDL models may be imported, compiled and simulated with no modification, and furthermore the available test models are written in VHDL. It should be noticed that the ICEM proposal allows the designer to specify the equivalent generator quoted above as a VHDL-AMS description. Therefore, it seemed that the VHDL-AMS language was best suited to our application.

Consequently, this paper introduces another technique, based on mixed-level (behavioural and structural) simulation, which may eventually reduce CPU times in a significant way, while preserving enough accuracy to meet the goals of an EMC-oriented study.

2 The methodology

From what has just been stated, we can suggest a 3-step process in order to model the equivalent supply current generator of a microcontroller.

The equivalent supply current $I_b$ is composed of several currents consumed by the core, the Flash EEPROM and the SRAM. Simulation allows the designer to tell them apart, which is far more difficult to achieve by measurements.

The toolset used is ADVance-MS Mach from Mentor Graphics. ADVance-MS [3] is a VHDL-AMS tool based on the Eldo simulation core, which is very accurate but very slow for 100000-transistor netlists; on the contrary, Mach [2] is designed for million-transistor netlists and thus much faster (10 to 12 times), but at the expense of accuracy. ADVance-MS Mach is claimed to combine both cores in a unique environment.

At first, the current consumed by the core can be extracted by simulating the transistor-level core netlist under Mach. This netlist can be obtained after either the synthesis step (with active devices only) or the RC extraction step (with detailed parasitics depending on floorplanning and routing). Thanks to ADVance-MS, this SPICE-like netlist can be co-simulated with digital-only, VITAL VHDL models of the memory blocks by the means of "virtual" analog-to-digital and digital-to-analog converters specified in VHDL-AMS; in addition, a given executable code can be taken into account by the (E)(E)PROM model, driving data pins according to its contents. This process is depicted in figure 2.

Obviously, this simulation does not include the current consumed by the memory blocks, and thus must be compared with measurements in RESET mode, but is compulsory in order to validate the methodology and the tool.

The second step consists in performing an analysis of the current consumed by the memory blocks themselves, and then in writing a VHDL-AMS behavioural model of this current. Eventually, these models can be coupled with the core netlist in the same manner, thus giving the whole transient supply
current (figure 3) which can now be compared with measurements in RUN mode. Of course, previous VITAL models may be re-used as far as the digital behavioural part is concerned, since VHDL-AMS is upward-compatible. Finally, a behavioural VHDL-AMS model of the supply current can be written for the core as well; it can take into account the most current-consuming instructions of the microcontroller. This model can be interfaced with the purely digital VHDL model of the core, making it possible to use the whole setup as an "EMC advisor" in which the relationship between the executed machine code and the conducted emission can be examined. Since only behavioural models are now used (figure 4), simulation times can be reduced by 1000 times or more compared with previous setups.

3 Validation and results

3.1 Simulation with VITAL models

The validation of the methodology proposed above was carried out on a 8051 microcontroller core from Atmel (DIVA project), including a 32KB code EEPROM and 2 data SRAMs (1KB and 256B); the core represents about 25000 equivalent NAND gates, both SRAMs represent about 18000, and finally, the EEPROM alone represents more than 150000 ...

Previous research described in [5] proved the validity of the ICEM model in "low" frequency bands (below 2 GHz). Since lumped elements were perfectly measured and identified for our microcontroller, the predicted external current can be computed by simulating the core (represented by $I_b$) with these additional elements (described in the VHDL-AMS model), and thus these results can be correlated with external current measurements. It must be noticed that the internal equivalent capacitance $C_b$ is the sum of the metal capacitance (due to power supply rails) and the MOS capacitances (due to the transistors themselves); since the core netlist already includes the latter, only the metal capacitance is explicitly included in the simulation netlist.

Simulation results with 3 ns rise and fall times for the clock signal are displayed in figure 5 (left), in which $I_{int}$ represents the internal current and $I(RMEASC)_{1:4}$ the predicted external current. They can be compared with real-world measurements in figure 6: peak values are nearly the same in both cases, but the uncertainty on internal capacitances, as well as the absence of internal parasitic elements (resulting from the place-and-route step) in the simulated netlist, may partially explain the differences between both signals. Delay times depend on clock rise and fall times, as stated in Hirata’s work [4]; consequently, the internal clock generator plays an important role in the correlation between simulation and measurements. However, this simulation covers only the RESET state, and general rules may not be inferred from such a
short equivalent time. In addition to that, the effects of parasitic elements are not included at this time: due to gate switching desynchronisation, internal current peaks should then be wider than with the plain transistor netlist. A method for DSPF (Detailed Standard Parasitic File) import in ADVance-MS Mach is currently being investigated (compatibility issues between formats used by CAD tools).

Finally, a very simple VHDL-AMS behavioural model of the core was developed. Simulation results (figure 5, right) show a good correlation between the netlist and this model, seeing that the behavioural simulation is about 1000 times as fast.

3.2 Simulation with transistor-level memories

A quick structural simulation shows that, as far as the aforementioned microcontroller is concerned, the current consumed is much lower in the Flash EEPROM than in the SRAM: therefore, only the latter should be considered. The circuit used in this study is the 1280x8-bit 0.35 μm data SRAM block, composed of 4 blocks of 80 rows and 4 columns each. Therefore, 3 address decoders are used: a 7-bit row decoder (called X, most significant address bits), a 2-bit column decoder (Y) and a 2-bit block decoder (Z). More detailed information on such an architecture can be found in [10].

For each block, current peaks depend on the rise and fall times of input signals, as stated in [4]. Since the memory cells are activated by a specific control signal (Memory Enable), the dynamic current activities for the address decoders and the memory array can be studied separately. The following results are inspired by an interesting approach addressed in [7], but there limited to the computation of the total energy consumption.

In order to state this, the transistor-level netlist was driven by a VHDL digital testbench browsing every decoded address, as shown in figure 7). Transistor-level extraction was performed for many address sets; it clearly demonstrates previous assertions, i.e. that:

- the dynamic activity of memory cells in write mode depends neither on addresses nor on data
- the dynamic activity of address decoders is widely address-dependent, with a multi-peak PWL waveform

Another simulation showed that, by reducing transition times on address signals, address decoder waveforms tend to converge towards a unique peak, the amplitude of which can reach the same order of magnitude as the one associated with memory cells. This clearly indicates that address decoder activity can not be neglected when evaluating SRAM EMC compliance.

Since procedural descriptions are not implemented in ADVance-MS, the model
implements a linear interpolation algorithm, the coefficients of which are computed in "realtime" in a process for both decoders and for memory cells. Basic waveforms are encoded as real vectors, with an Eldo-like syntax, and for only one switching bit as far as address decoders are concerned. Then waveform computations are triggered within the process by transitions on addresses and select signals. Hamming distances are computed between the previous address and the current one, for both upward and downward transitions and both X and YZ decoders. The results act as multiplying factors for the current peaks generated by the Y and Z decoders. The X decoder waveform may interfere with Y and Z ones because of separate paths (i.e. propagation delays); obtaining the whole decoder waveform thus requires at least two separate processes, which still remain to be coded.

SRAM simulation results for different accesses using Y and Z decoders are then displayed in figure 8 (left), where the upper plot represents the transistor-level results and the lower plot the VHDL-AMS behavioural model results. The results show a good correlation between both simulations, including peak values for address decoders, quoting that the behavioural-level simulation is about 1000 times as fast as the transistor-level one (as already noticed for the core).

At the time this paper is written, the address decoder is partially modelled (only Y and Z decoders), the memory cells in write mode are entirely modelled, including the influence of rise and fall times. The X decoder is under study, and the influence of memory contents in read mode still remains to be investigated (but preliminary simulations show it is very limited).

Figure 8 (right) illustrates the predicted external current due to the SRAM block, using the same passive power supply network as in core simulations. It is thus clearly stated that, in this class of 8-bit microcontrollers, SRAM activity has hardly any influence on the external current (2.5 mA versus 30 mA peaks), which is correlated by preliminary simulations, but this may not be the case as far as 32-bit microcontrollers are concerned.

4 Conclusion and perspectives

This paper suggests a methodology for extracting, modelling then predicting power supply currents in a microcontroller by using mixed-mode simulation. For this purpose, the use of the VHDL-AMS language, permitting high-level memory modelling, is proposed.

This methodology is currently under validation by measurements performed on the core. However, the results obtained on SRAM blocks show the feasibility of a dynamic current consumption macromodel.

Memory activity does not represent a substantial part of the current consumed by simple (8 or 16-bit) microcontrollers; however, more complex (32-bit
then 64-bit) microprocessors and microcontrollers always include SRAM cache memories, which are accessed at every clock cycle or so. Furthermore, asynchronous SRAMs have been replaced by synchronous ones, which are faster and more perturbating. Consequently, embedded memories should play more important a role in the total consumption of those high-performance devices. One of the main advantages of behavioral models, apart from their reduced simulation times, lies in the fulfillment of confidentiality demands. Behavioral ICEM models of integrated circuits, described in VHDL-AMS and including the passive elements and the current generator, can be supplied to system designers, allowing them to study EMC compliance at board level without revealing internal architectures. Such a methodology may be applied to other IC pins as well, knowing that a recent IBIS (Input/output Buffer Information Specification) proposal, namely IBIS-ML (Macro-Language), supports (among others) the use of VHDL-AMS models. Consequently, such models may lead to the definition of a generic "ICEM-IP" (Intellectual Property) model, providing guidelines for EMC-oriented design.

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References


Fig. 1. The ICEM model for power supply lines

Fig. 2. Simulation setup with VITAL memory models

Fig. 3. Simulation setup with VHDL-AMS memory models
Fig. 4. Simulation setup with full VHDL-AMS models

Structural: internal (top) and external (bottom)
Behavioural: internal (top) and external (bottom)

Fig. 5. Simulation of the core in the RESET phase
Fig. 6. Current measured in the RESET phase

Fig. 7. Setup for transistor-level SRAM simulation
Internal current, structural (top) and behavioural (bottom)

Internal (top) and external (bottom) currents

Fig. 8. SRAM simulation results