ICEM Modelling of Microcontroller Current Activity

Jean-Luc Levant\textsuperscript{a,}\textsuperscript{*}, Mohamed Ramdani\textsuperscript{b} and Richard Perdriau\textsuperscript{b}

\textsuperscript{a}ATMEL - La Chantrerie - Route de Gachet - 44000 Nantes - France  
\textsuperscript{b}ESEO - 4, rue Merlet-de-la-Boulaye - BP 926 - 49009 Angers Cedex 01 - France

Abstract

Better prediction of electromagnetic compatibility (EMC) for components is becoming a topical demand, due to technology improvements. It is requested by integrated circuit (IC) manufacturers as well as by equipment integrators. The French UTE standardisation group has proposed an EMC modelling methodology for ICs, called ICEM (Integrated Circuit Electromagnetic Model). This proposal improves and extends the IBIS standard towards conducted emission prediction (and later radiated emission) by providing additional information modelling the power network and the dynamic current activity of an IC, thus allowing the chip manufacturer to justify the package used as well as the number of power supply pins, and the equipment manufacturer to tune power supply and decoupling networks.

After a brief introduction to the ICEM model and the associated methods, this article shows a way of obtaining dynamic current activity models by measuring the current consumed on the IC power supply pins. The use of ICEM for the optimisation of decoupling networks, the evaluation of power supply noise and the tuning of the surface of power and ground planes is presented for the first time with subsequent results.

Key words: Electromagnetic compatibility, ICEM, measurement, modelling, simulation

* Corresponding author. Tel. (33/0) 2 40 18 18 77  
Email address: jean-luc.levant@nto.atmel.com (Jean-Luc Levant).
1 Introduction

According to the MEDEA+ EDA roadmap [5], despite ever decreasing supply voltages (0.3 V in 2013), conducted emission levels of integrated circuits should slightly increase (100 µV in 2013, with 25 GHz system clock, instead of 90). Therefore, predicting conducted-mode emission is an ever growing demand for future generation circuits.

This prediction relies on the knowledge of the current flowing in the power supply networks of an IC and its PCB. In order to obtain this current, the behaviour of the power supply network impedance and the profile of the instantaneous current consumed by the chip core both have to be identified. Each building block of the IC architecture (core, memories, buffers, analogue functions) can be modelled this way. ICEM [4] proposes a methodology dedicated to obtaining these models; they can be elaborated either within the design phase or from measurements on the working silicon.

Figure 1 depicts the main principles of ICEM modelling in the case of a microcontroller, including core and buffers. The core and buffer models include the power supply impedance as well as a specific current activity (RESET mode, memory accesses ...). An isolation resistance between both grounds represents the substrate leakage resistance and is supplied by the model as well. Of course, depending of the IC, each entity can have its own ICEM model.

The ICEM methodology can be used either within the IC design phase or with measurements on an existing chip; both approaches are displayed in figure 2. Only the measurement-based approach is introduced in this article: the transfer function of the power supply network is characterized in frequency domain from measurements, then it is coupled with time-domain measurements of the external current, in order to obtain a time-domain representation of the internal current. In addition to that, a methodology to compute the predicted external current from the simulated internal one is under development and validation [3].

2 Obtaining the ICEM model from measurements

This approach consists in modelling the power supply network and the dynamic current for a given activity. This article introduces an original methodology for both modelling steps. An 8-bit microcontroller from the 80C51 family is chosen as a demonstrator.
2.1 Power supply model of the microcontroller

In order to obtain the dynamic current activity model, the first step consists in determining which elements (RLC, transmission lines) should be used to model the power supply network impedance; for that purpose, the rise time of the current flowing in this network as well as the length of the associated path should be known. Figure 3 depicts the evaluation of the critical dimensions of this path.

The whole distance $L$ covered by the current between VDD and VSS is $2 \times 13.45$ mm, namely 2.69 cm. The critical electrical length $l_{\text{critical}}$ of this path, below which the transmission-line based mode should be used is, for an 8-ns $t_r$ rise time:

$$l_{\text{critical}} = \frac{t_r v_p}{6} = \frac{8 \times 10^{-9} \times 152.10^6}{6} = 20 \text{ cm}$$

(1)

where $v_p$ is the mean propagation speed in the substrate, a plastic package with a $\epsilon_r$ dielectric constant equal to 3.9:

$$v_p = \frac{c}{\sqrt{\epsilon_r}} = \frac{3.10^8}{\sqrt{3.9}} = 152.10^6 \text{ m.s}^{-1}$$

(2)

The quarter-wave length of this connection where the first resonance appears is 5 cm; consequently, the physical length of the supply connection ($L=2.69$ cm) is far lower than the quarter-wave (5 cm). As a result, a lumped-element (RLC) model is accurate enough to model the power supply network. These RLC elements are extracted from measurements using a vector network analyser [1], as depicted in figure 4. The bandwidth capable of dealing with this rise time is:

$$F_{\text{max}} = \frac{0.35}{t_r} = \frac{0.35}{8 \times 10^{-9}} = 250 \text{ MHz}$$

(3)

Harmonics above this frequency are considered low enough not to generate noticeable emission levels; $F_{\text{max}}$ is thus the frequency limitation for our model. A test board is directly connected to the analyser, and should be modelled as well in order to distinguish between the IC and the test environment itself.

Figure 5 demonstrates that the test board model is obtained thanks to the network analyser, by grounding the inner conductor of the SMA connector. The model is in fact a RL network composed of a $0.044 \Omega$ resistor and a $0.34 \text{ nH}$ inductor. The board used in this study is 0.5 mm thick.

Figure 6 illustrates an example of power supply pin pair modelling. The VSSC1 pin is grounded (test board ground) and the VDDC1 pin is connected to the inner conductor of the SMA connector. The frequency response of the
impedance up to 300 MHz can be divided into three parts. Under 10 MHz, the impedance is capacitive and its value can be computed at a given frequency. At 15 MHz, it becomes resistive and its value is read on the plot. Above 20 MHz and until 300 MHz, the impedance is inductive and can be computed as well at another given frequency. Figure 7 represents the partial model of the power supply network for this pair.

The same methodology is used for every power supply pair (core and buffers).

2.2 Current activity model of the integrated circuit

The modelling methodology relies on the measurement of the external current consumed by the IC [2]; figure 8 shows the measurement and acquisition chain. This measurement is achieved by inserting a resistor ($R_m$) in the power supply rail and plugging a differential probe across it; $R_m$ must be low enough to generate only a small supply voltage drop (<100 mV). In this example, three differential probes help rebuilding the external current ($I_{ext}$); then the scope directly performs the addition of the three measurements. The results are saved in text format, usable by the processing algorithm written in Matlab.

In order to obtain the consumed current model, a given activity must be defined; in this example, the RESET mode of the microcontroller is chosen. The general principle relies on the knowledge of the power supply network as well as of the measurement of the external current consumed by this network, as depicted in figure 9. The equivalent $I_{int}$ current flows into two parallel branches; measuring $I_{ext}$ leads to $I_{int}$ by determining the transfer function $K_z(f)$:

$$I_{int} = I_{ext} \cdot K_z(f) \quad \text{where} \quad K_z(f) = \frac{R_m + Z_1 + Z_2}{Z_2} \quad (4)$$

In order to achieve this principle, the time-domain current $I_{ext}(t)$ must be converted into the frequency domain $I_{ext}(f)$ thanks to a FFT. Then the product $K_z(f) \cdot I_{ext}(f)$ yields the internal current $I_{int}(f)$. An inverse FFT converts $I_{int}(f)$ back into the time domain $I_{int}(t)$. The methodology is explained in figure 10.

In order to preserve model accuracy, appropriate time and frequency resolutions for the measurements must be correctly defined. Internal currents can be observed during several microseconds (which depends from the chosen activity) while having transitions times as low as 1 ns.

These criteria define the electrical characteristics of the scope dedicated to $I_{ext}(t)$ acquisition. Modelling the activity in RESET mode requires a 4 µs acquisition time, a 100 ps time resolution (10 points in each transition) and, consequently, a 40 Kbyte trace depth. The acquisition chain is composed of 1.7 GHz differential probes and a 4 GHz oscilloscope. The whole bandwidth
is thus:

\[ B_{\text{tot}}(\text{GHz}) = \sqrt{\frac{1}{1.7^2} + \frac{1}{4^2}} = 1.56 \text{ GHz} \]

(5)

The sampling frequency of the scope is 10 GHz: easily high enough to assure accurate measurements. Moreover, it is mandatory to check out that sampling-induced noise does not affect measurements; should it be the case, an anti-aliasing filter must be included in the acquisition chain. Lowpass filters integrated in some oscilloscopes enable to fit their bandwidth to the observed signal.

Figure 11 displays both the measured current \( I_{\text{ext}}(t) \) and the internal current \( I_{\text{int}}(t) \) extracted thanks to this method. The internal current flowing into the IC is much higher than the external one (150 mA versus 7 mA peaks); the power supply network is responsible for filtering.

Figure 12 shows a significant correlation between the external current regenerated by the FFT/IFFT method and the measured one.

3 ICEM model use

3.1 Noise estimation on power supplies

The full ICEM model of the IC is depicted in figure 13. The core as well as the buffers are modelled along with the test board (SMA connector and PCB). \( I_{\text{intC}} \) and \( I_{\text{intB}} \) represent the current activity models in RESET mode.

The power supply model and the current profile enable the measurement of the supply noise (on VDDC). Figure 14 shows a good correlation between the simulated noise and the measured one; the model should be improved in order to refine the prediction.

3.2 Decoupling network optimisation

Another possible use is the optimisation of the decoupling network. As an example, four decoupling capacitors were added to the previous model in order to lower the impedance of the power supply network in the frequency band of interest. Figure 15 demonstrates an excellent correlation between the simulated network and the measured one.

Of course, the model of the decoupling capacitors must be determined; subsequent information is often provided in data books. In our case, the models were measured with the network analyser, in order to state the limits of the
ICEM approach. The results prove that accurate modelling easily provides enough accuracy to meet the goals of EMC analysis: in this example, it can be noticed that the 10 nF capacitor has hardly any influence and could then be omitted.

3.3 Influence of ground and power planes

The ICEM model could be used as well for evaluating and optimising the surfaces of ground and power planes. They act as efficient decoupling capacitors in high frequency due to their low ESR and inductances. Figure 16 shows their influence on the impedance profile.

The decoupling capacitance associated to ground and power planed depends on surface, thickness and dielectric. Its value is given by the following formula:

\[ C = 8.85 \varepsilon_r \frac{A}{d} \quad (pF) \]  

where \( \varepsilon_r \) is the dielectric constant (4.9 for FR4 epoxy), \( A \) the surface \( (m^2) \) and \( d \) the distance \( (m) \) between both planes. For a 25 cm\(^2\) wide, 0.5 mm thick plane, the capacitance reaches 217 pF. Figure 16 shows that both planes compensate for network antiresonance around 400 MHz.

4 Conclusion

The ICEM methodology relies on the description of two submodels: the power supply network and the dynamic current bound to a specific activity. This article shows that accurate modelling of the network and the internal current is made possible without too many complications. In addition to that, it proves that both models are accurate enough to evaluate noise levels of power supplies, to optimise the decoupling networks (number and values of capacitors) as well as to predict the surface of copper planes up to 300 MHz. Another use, which is not considered here and is bound to more accurate knowledge of the current flowing on the board, is the prediction of conducted and radiated emission levels of the IC and its associated PCB. The ICEM model is being currently validated in these application fields, and the first results are really encouraging. Furthermore, new models, based on transmission lines, are being studied for UHF frequency bands above 300 MHz; promising results should be eventually published.
References


Fig. 1. ICEM modelling principle

Fig. 2. Different approaches for ICEM generation

Fig. 3. Path length from VDD pin to VSS pin
Fig. 4. Measurement setup used to extract the elements of the power supply network model

Fig. 5. Model of the test setup: a resistor and an inductor

Fig. 6. Power network impedance measured between VDDC1 and VSSC1 pins
Fig. 7. Example of power network impedance for a power supply pair

Fig. 8. Measurement and acquisition chain

Fig. 9. Internal current extracted by using the $I_{ext}/I_{int}$ transfer function

Fig. 10. Modelling principle for IC current activity
Fig. 11. Current profile extracted by the ICEM method

Fig. 12. Comparison between simulation and measurements
Fig. 13. Full ICEM model of the microcontroller

Fig. 14. Noise on VDDC pin
Fig. 15. Impedance of the decoupled power supply network: measured (left) and simulated (right).

Fig. 16. Influence of ground and power planes on the impedance profile.