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Comparison among emission and susceptibility reduction techniques for electromagnetic interference in digital integrated circuits

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1. Introduction

Within the recent years, digital and analog integrated circuits (ICs) have been developing using a very small channel length (nanometer technology), with an increase in operating frequency and interface numbers as well as a decrease in node capacitance, power supply voltage and, consequently, noise margin. Therefore, these ICs are becoming more and more susceptible to the electromagnetic interference (EMI) induced by other ICs, antennas and, more generally, telecommunication systems. They also represent emission sources which can easily disturb other circuits located either on the same board or other boards. Therefore, a properly designed IC must bear both a low emission level and a high immunity level (i.e. ability to withstand EMI without exhibiting any malfunction). However, it may not be possible to meet both constraints at the same time.

Several measurement methods have been developed, some of them standardised, to characterise the electromagnetic emission and susceptibility of ICs. The most commonly used are summarised in Table 1.

In this paper, two of the aforementioned measurement methods (direct power injection, DPI and near-field scanning, NFS) are actually used to establish a comparison among emission levels and immunity levels of several IC cores using different power supply architectures, originally intended for emission reduction. Likewise, the susceptibility of the same IC against electrostatic discharge (ESD) is assessed using the very-fast transmission-line pulsing (VF-TLP) technique. The objective of this study is to check out whether these reduction techniques are also valid for susceptibility reduction, as well as to classify them according to their respective efficiencies and costs.

The paper is organised as follows. First of all, the different logic cores of the test chip used in this study are described in Section 2. Then, immunity measurement methods are detailed in Section 3, with an emphasis on their set-ups and their results. Section 4 deals with emission measurements. Finally, Section 5 underlines the key points of this study and opens to future research in the immunity of mixed-signal circuits.

2. Description of the test chip

The test chip used in this study, called CESAME \textsuperscript{[9]}, has been developed by STMicroelectronics in 0.18 \textmu m CMOS technology (die area: 11 mm\textsuperscript{2}), specifically for the investigation of several EMI
reduction techniques [10]. CESAME is composed of six logic cores which are identical from a functional point of view, but only differ by their power supply strategies. Each core is composed of 240 identical base cells, each one including D flip-flops, a clock tree and standard gates, intended to reflect the activity of a typical digital core. These cores are built on an epitaxial substrate with a negligible horizontal resistance.

In this paper, three cores out of the six are studied (Fig. 1).

**NORM core**: The only EMI protection strategy used in the NORM core consists of two small 1.7Ω series resistors, one on each power supply rail. These resistors, along with the metal and MOS capacitances of the logic core, build up a RC filter, with a high cutoff frequency (about 200 MHz).

**ISO core**: Another protection strategy is used for the ISO core. This core is embedded in its own local substrate, isolated from the rest of the chip thanks to a triple-well technique (Fig. 2).

**RC core**: In this core, an additional 1 nF integrated decoupling capacitor is included between both supply rails (Fig. 3). This distributed on-chip capacitor is made up of several poly1/poly2 capacitors, and increases the area of the RC core by 40% compared with the NORM core. By lowering the cutoff frequency of the RC filter (about 40 MHz), this technique allows the reduction of the

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**Table 1**
Summary of immunity and emission measurement methods for integrated circuits

<table>
<thead>
<tr>
<th>Method</th>
<th>Upper limit (GHz)</th>
<th>Type</th>
<th>Immunity</th>
<th>Emission</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Ω/150Ω</td>
<td>1</td>
<td>Conducted</td>
<td>No</td>
<td>Yes [1]</td>
</tr>
<tr>
<td>Bulk current injection (BCI)</td>
<td>1</td>
<td>Conducted</td>
<td>Yes [4]</td>
<td>No</td>
</tr>
<tr>
<td>Direct power injection (DPI)</td>
<td>1</td>
<td>Conducted</td>
<td>Yes [5]</td>
<td>No</td>
</tr>
<tr>
<td>Transverse electro magnetic (TEM) cell</td>
<td>1</td>
<td>Radiated</td>
<td>Yes [6]</td>
<td>Yes [7]</td>
</tr>
<tr>
<td>Near-field scanning (NFS)</td>
<td>6</td>
<td>Radiated</td>
<td>Yes</td>
<td>Yes [8]</td>
</tr>
</tbody>
</table>

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**Fig. 1.** CESAME test chip and the three cores under test (NORM, ISO and RC) surrounded in red.

**Fig. 2.** Comparison between NORM and ISO core architectures.
3. Immunity measurements

In this paper, two different injection methods (DPI and VF-TLP) are successively used in order to measure the immunity of the CESAME IC to either EMI or ESD disturbances, as well as to assess the efficiency of the aforementioned techniques. Both techniques use the same injection set-up (based on the DPI standard) but very different stimuli, thus making it possible to evaluate the behaviour of the IC to either continuous-wave or transient interference.

3.1. Immunity criterion

Every susceptibility study must define a criterion that the IC should meet to be considered immune to EMI or to ESD for a given aggression. In this experiment, an ubiquitous criterion is used: a failure in the IC is characterised by the ripple of the output signal reaching 20% of its nominal voltage level, or by the jitter of this output signal reaching 10% of the period. Moreover, another criterion is added for the VF-TLP method, in which the circuit is considered immune depending on the percent of logical errors triggered during pulse injection.

3.2. Direct power injection (DPI)

3.2.1. Description

The DPI method has been standardised under the supervision of the international electrotechnical commission (IEC) [12]. An example of a DPI set-up is displayed in Fig. 4.

Continuous sine-wave RF power (from 10 MHz to 1 GHz) is fed into an amplifier and then injected into a pin of the IC under test (which could be either a power pin or a signal input pin) through a capacitor blocking the DC voltage coming from the power supply (hence the name of the test) [13]. A directional coupler allows the measurement of incident and reflected powers by the means of two power meters. The IC under test works under normal operating conditions (20 MHz clock frequency), and the data output of the circuit under test is connected to an oscilloscope (adapted to 1 MΩ) through a 1 MΩ passive probe, which makes it possible to observe a malfunction of the circuit during the experiment.

The measurements described in this article are performed while injecting power into the global substrate of the test chip (via the Vss power pin), which proved to be a valuable experiment [13]; moreover, since the substrate of the IC is epitaxial, it can be considered that the perturbation propagates in the same manner towards each core.

The transmitted power $P_{\text{trans}}$ to the whole device under test (DUT) can then be expressed from the measured incident power $P_{\text{inc}}$: $P_{\text{trans}} = (1 - |S_{11}|^2)P_{\text{inc}}$. (1)

where $S_{11}$ is the reflection factor and $P_{\text{inc}}$ the incident power delivered by the generator. This reflection factor was measured thanks to a vector network analyser (VNA) [14].

By replacing the reflection factor by its expression, the following is obtained:

$$P_{\text{trans}} = \left(1 - \frac{Z_{\text{DUT}} - Z_0}{Z_{\text{DUT}} + Z_0}\right)^2 P_{\text{inc}}.$$ (2)

where $Z_{\text{DUT}}$ is the impedance of the DUT and $Z_0$ the characteristic impedance of the sine-wave generator (50 Ω). By separating the real and imaginary parts of $Z_{\text{DUT}}$, the exact expression of the transmitted power (i.e. the power entering the DUT) can be obtained:

$$P_{\text{trans}} = \frac{4Z_0\text{Re}(Z_{\text{DUT}})}{Z_{\text{DUT}} + Z_0^2} P_{\text{inc}}.$$ (3)

The expression in Eq. (3) is well suited to the calculation of $P_{\text{trans}}$ from measurements, owing to the use of power meters in DPI experiments. In this case, the DPI experiment consists in injecting continuous power into the substrate pin of the NORM core. Since
this core is implemented in the global substrate of the IC, the injected power is dissipated in the whole substrate. This substrate noise has an influence, not only on the NORM core itself, but also on the other cores implemented inside the circuit.

3.2.2. Results

DPI measurements were performed from 10 MHz to 1 GHz in 10 MHz frequency steps. For each frequency, the injected power (i.e. the power delivered by the generator) at which the IC becomes susceptible was recorded. The whole frequency plot is represented in Fig. 5 for the three cores.

The deep N isolation layer between the global substrate and the local substrate of the ISO core (Fig. 2) lowers the coupling capacitance between both substrates. Hence, it can be seen that the susceptibility of the ISO core is generally lower than the one of the NORM core, particularly from 10 to 210 MHz. However, it can be noted that the ISO core is less immune than the NORM core between 400 and 500 MHz; this may be due to an antiresonance of the coupling capacitor with the passive elements of the power supply network.

The RC core (Fig. 3) includes an on-chip decoupling capacitor between the $V_{dd}$ and $V_{ss}$ power supply rails. This on-chip decoupling capacitor enhances the immunity of the RC core in comparison with the others, except between 500 and 650 MHz where the RC core is less immune than the ISO core; likewise, an antiresonance of the capacitor with the power supply network may explain this behaviour. In high frequency (above 650 MHz), the ISO and RC cores have similar susceptibility levels except at 780 MHz.

3.3. Very fast transmission line pulsing (VF-TLP)

3.3.1. Purpose

An ESD is the sudden and momentary electric current that flows when an excess of electric charge stored on an electrically insulated object finds a path to an object at a different electrical potential (such as ground), which may cause damage to electronic equipment.

At the time being, there is no ESD test dedicated to the characterisation of the immunity of ICs. Moreover, the only system-level test is described in the IEC 61000-4-2 standard [15]: an ESD gun is used to inject a disturbance into the input/output pins of a printed circuit board (PCB) in order to ensure ESD safety (namely, no destruction). The steep decrease of oxide thickness in transistor gates increases IC susceptibility to ESDs which are likely to occur in complex environments (automotive), where ESDs can be triggered even while the system is on. This can lead to system-level failures like spurious resets, erasures of memory contents, or logic level mismatches equivalent to EMC susceptibility effects.

ESD phenomena are represented by several models depending on the kind of electrostatic source:

- The Human Body Model (HBM) simulating the discharge of a human being onto an electronic device: unique pulse with
2–10 ns rise time, 130–170 ns time delay, and 0.25–0.30 A peak current for a 400 V voltage.

- The Machine Model (MM) simulating the discharge of metallic equipment onto a grounded electronic device: damped 12 MHz sine-wave signal with 6–8 ns rise time and 4.6–7.0 A peak current for a 400 V voltage.
- The Charged Device Model (CDM) representing the self-discharge of a charged IC through its package: unique pulse with 300–500 ps rise time, 0.5–1.5 ns time delay, and 1.7–2.5 A peak current for a 400 V voltage.

In particular, the CDM is well-suited to IC immunity testing [16] due to the frequent advent of such events in product assembly lines. However, CDM tests only provide “pass–fail” results which do not output any information about the behaviour of the circuit under test. Therefore, the VF-TLP method [17] was designed as a characterisation tool of the dynamic behaviour of the circuit under test under a CDM stress. It consists in injecting very fast square current pulses (with a rise time lower than 500 ps and a width between 1.25 and 10 ns) through a transmission line, by the means of a high-power time-domain reflectometer (TDR), and extrapolating voltages and currents related to the DUT through the measurement of incident and reflected pulses. Basically, the VF-TLP test is traditionally used to characterise I/V protections of ICs. Conversely, in this approach, it is used to inject a ESD-like disturbance on a IC under operation [18].

### 3.3.2. Measurement method

In this study, the VF-TLP signal is fed into the $V_{ss}$ pad of the active circuit under test by an injection probe and a 1 nF injection capacitor, in order to mimic the DPI measurement setup as closely as possible. Fig. 6 illustrates the VF-TLP measurement setup with the injection system and the DUT. It includes a 4-channel digital oscilloscope with selectable input impedance.

The 3-way TDR box of the VF-TLP system makes it possible to visualise the incident and reflected pulses injected into the DUT. The input signal of the TDR box is viewed on a 50 $\Omega$ input of the oscilloscope through a coaxial cable; the main output signal of the TDR box is connected to the injection probe, while the third port of the box is connected to another 50 $\Omega$ input of the oscilloscope, making it possible to observe incident and reflected pulses. Finally, the data output of the circuit under test is connected to the third input of the oscilloscope in the same manner as for the DPI test. As far as VF-TLP is concerned, the same criterion is used, but the measurements performed are of course different. Variable-amplitude pulses are injected into the substrate of the NORM core, with a 180 ps rise time and a 5 ns width. This pulse flows towards the output signal through the coupling path. The circuit becomes susceptible when the peak amplitude of the resulting pulse reaches the criterion, that is 0.4 V.

#### 3.3.3. Results

VF-TLP measurement results are illustrated in Fig. 7. It can be seen that the NORM core is already susceptible at a 20 V pulse amplitude, while 30 V are required to disturb the operation of the ISO core. The RC core is less susceptible: logic errors appear at the output of the RC core only when the amplitude of the injection pulse reaches 40 V. Finally, this shows that the NORM core is the least immune, followed by the ISO core and finally the RC core.

It is also interesting to notice that the immunities of both NORM and ISO cores are identical above 30 V. This may be due to the parasitic conduction of the (theoretically) reverse-biased junction made up of the triple well and the local substrate of the ISO core, due to the high amplitude of injected pulses.

To confirm these results, another VF-TLP test was then performed: a series of 100 pulses with a 70 V amplitude (hence, higher than the susceptibility levels of all cores) were injected into the substrate, then, the logic errors induced in the output of each core by these pulses were visualised and counted. Table 2 shows the percentage of logic errors for each core.

It can be noticed that this test confirms the classification already established for the three cores. The logic behaviour of the output signals of the three cores will then be investigated accurately in future studies for power and pulse injection into the substrate and the power supply rails of these cores.

### 4. Emission measurement

#### 4.1. Measurement method

For several years, the NFS technique has been used in different fields like medical scanning, antenna analysis [19] and currently...
hot spot scanning of VLSI devices [20–22]. In the IEC61967-3 standard [12], this technique makes it possible to measure electromagnetic emission induced by an IC and the PCB on which it is mounted. This measurement allows the optimisation of the internal power distribution network of the IC as well as its floorplan. Moreover, it is easy to set up and does not require the implementation of specific PCB circuitry unlike, for example, the $1\Omega/150\Omega$ measurement method for conducted emission [12].

The whole scanner is made up of a mechanical 3D robot, a controller with its supervision system (PC), some measurement probes, a pre-amplifier and a spectrum analyser (Fig. 8).

The controller is used to drive the 3D robot along the three X, Y and Z axes, thus allowing the measurement of the corresponding fields ($E_x$, $E_y$, $E_z$, $H_x$, $H_y$ and $H_z$) using different probes. These probes (monopole, dipole and loop antenna) ensure a good cross-polarisation level and a high enough electric to magnetic field rejection [23]. The mechanical 3D robot of the near-field scanner enables a reproducible positioning of the probes above the circuit under test with high accuracy (0.5 mm steps at best resolution). The low magnitude of each field requires the use of a pre-amplifier (25 dB gain) between the probe and the spectrum analyser. For each mechanical scanning step, a spectral analysis is performed in synchronisation with the controller (Fig. 8).

In this study, the measurement of the normal component of the magnetic field ($H_z$) is achieved thanks to a loop probe made up of coaxial cable (internal diameter: 1 mm) and located at 1 mm above the circuit under test, either perpendicular or parallel to the package. Scanning is performed on top of the circuit within a 40 mm wide square, with a 0.2 mm step size, and at 50 MHz. However, processing was limited to a 25 mm wide square, namely, the package itself. In the same manner as for susceptibility measurements, the three cores are activated separately. Such measurements had already been performed by Tankielun et al. [10], except on the ISO core.

### 4.2. Results

Measurement results for the normal ($H_z$) component of the magnetic field are plotted in Figs. 9–11 for each of the three cores under test (NORM, ISO and RC), while Table 3 summarises their peak values.

It is clearly visible that the RC core is the least emissive (by 10 dBm compared with the NORM core), followed by the ISO core and, finally, the NORM core, which demonstrates the efficiency of the reduction techniques implemented into the RC and ISO cores, which are based on different principles. The low-pass filter made up of the integrated decoupling capacitor of the RC core and the parasitic elements of the passive power supply network of the chip attenuates harmonics in high frequency. Conversely, the limitation of substrate coupling in the ISO core is responsible for the limited propagation of substrate noise into this core.

![Fig. 7. Comparison among the immunities of the NORM, ISO and RC cores using the VF-TLP injection method.](image1)

**Table 2**

<table>
<thead>
<tr>
<th>Core</th>
<th>Pulse amplitude (V)</th>
<th>Width (ns)</th>
<th>% of logic errors</th>
</tr>
</thead>
<tbody>
<tr>
<td>NORM</td>
<td>70</td>
<td>5</td>
<td>9</td>
</tr>
<tr>
<td>ISO</td>
<td>70</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>RC</td>
<td>70</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

![Fig. 8. Near-field scanner setup.](image2)
5. Comparison between immunity and emission results

From the measurement results described in the previous sections, an interesting result lies in the immunity ranking of the three cores, which is the exactly the same for both aggression techniques (continuous-wave DPI and transient VF-TLP). Moreover, this ranking is also valid for emission. Table 4 summarises these results. The conducted emission results cited in this table were obtained by Tankielun et al. [10], unfortunately only for NORM and RC cores.

This classification demonstrates that the integrated decoupling capacitor seems to be the most efficient protection method to decrease both the susceptibility and the emission of digital cores. Nonetheless, the implementation of an isolation layer (ISO core), while not increasing the size of the die significantly, limits substrate coupling and leads to clean field cancellation on supply pairs.

Various authors [24] have investigated the influence of substrate noise reduction techniques on circuit performance. They advise to increase the resistivity of the global substrate in order to decrease the substrate noise by the addition of an external resistance, or increase the resistivity of a given region of the substrate. This last solution is costly and difficult, however, the existence of this multiple resistivity favours the implementation of many mixed-signal devices on the same substrate.

As far as the RC protection method is concerned, most multi-chip modules (MCMs) rely on surface mount capacitors for decoupling [25,26]. However, surface mount devices are bulky and have large parasitics which reduce their efficiency. Therefore, the interest of embedded capacitors for low emission has already been addressed in [11]. This study confirms that the low emission design rules edited in these previous papers are valid for high immunity as well: whenever possible, the integrated decoupling capacitor technique should be adopted.

6. Conclusion

This article presents several measurement results dealing with the susceptibility and emission levels of three identical digital cores with different power supply strategies. Both immunity tests applied in this paper (DPI and VF-TLP), as well as near-field emission scanning, demonstrate that the integrated decoupling capacitor seems to be the best solution to improve immunity while decreasing parasitic emission at the same time. However, this technique is expensive due to the significant increase in die area; therefore, many studies are focused on the development of new cost-effective integrated capacitors with small area and low parasitics.
In case this solution cannot be implemented, this paper also shows that the implementation of a triple-well isolation layer is a valuable improvement, yet less efficient than the integrated capacitor, to both the immunity and the emission of an IC (5–10 dBm in DPI and 10 V in VF-TLP for immunity, 3 dBm for emission).

In the future, near-field injection will be applied to the same cores in order to extend this study to the case of radiated immunity, and another test chip will be specifically designed and fabricated, with several analog and digital integrated blocks and new shielding methods, in order to study the efficiency of these techniques on external and internal immunities.

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References


